



Chip-Scale Energy and Power... and Heat

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Flexibility for Ultra Low Power

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Sub-threshold ($V_{DD} < V_T$) Survey

- Sub-threshold benefits
 - Leakage Power Decreases: 5X to 90X
 - Energy Consumption Decreases: 10X to 20X
 - E_{total} /operation minimized in sub- V_T
 - Aging Effects Improve: NBTI, EM, TDDB
- Challenges
 - Lower $I_{\text{on}} / I_{\text{off}}$
 - Variation
- State of art
 - Logic, SRAM, arithmetic units, processors, simple systems

Key Remaining Problems for Sub-threshold Operation in Systems

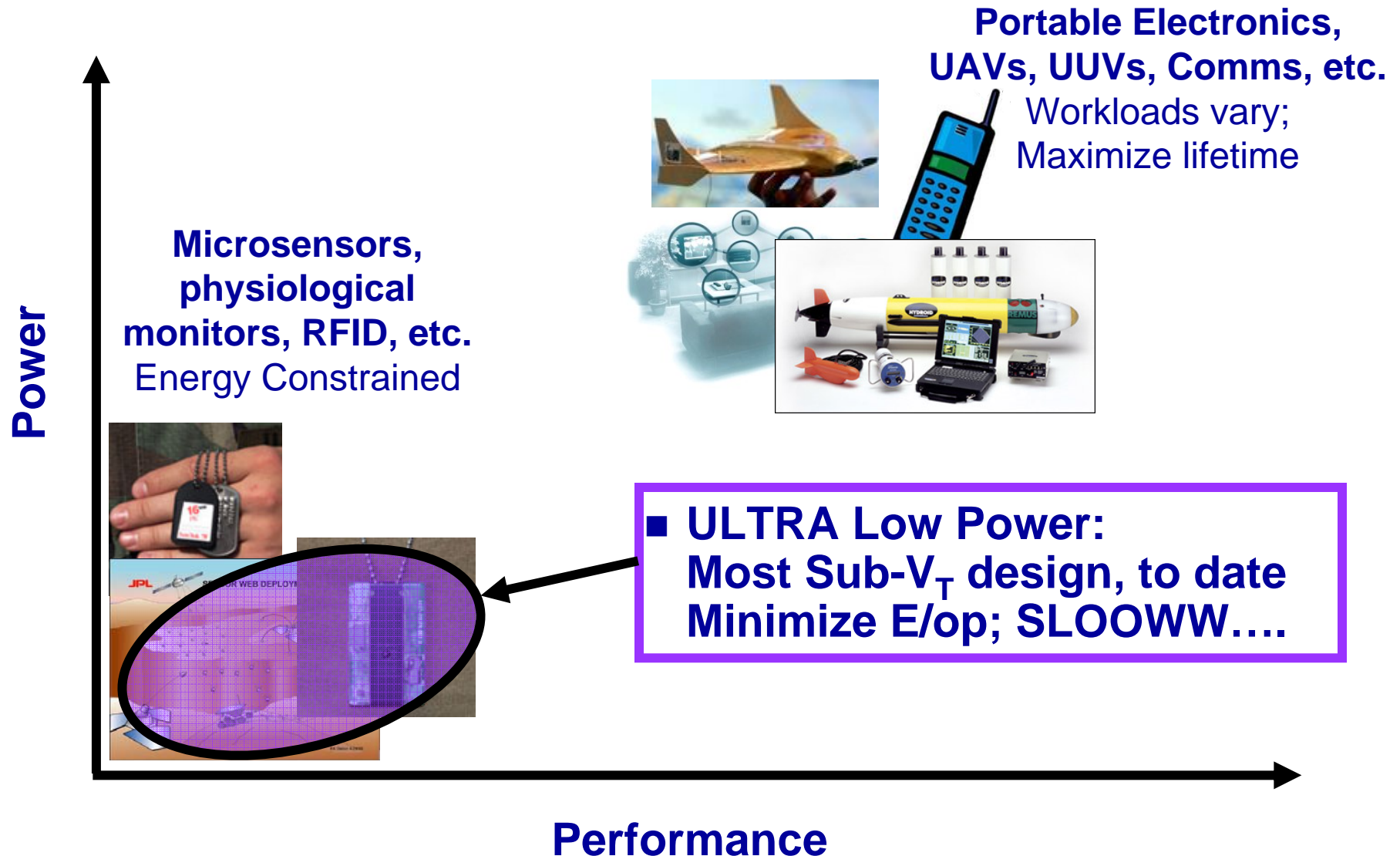
1. Very slow
2. Best efficiency comes from ASIC, but costly and slow for new applications
3. Digital power a small piece of pie in many ULP systems

Outline

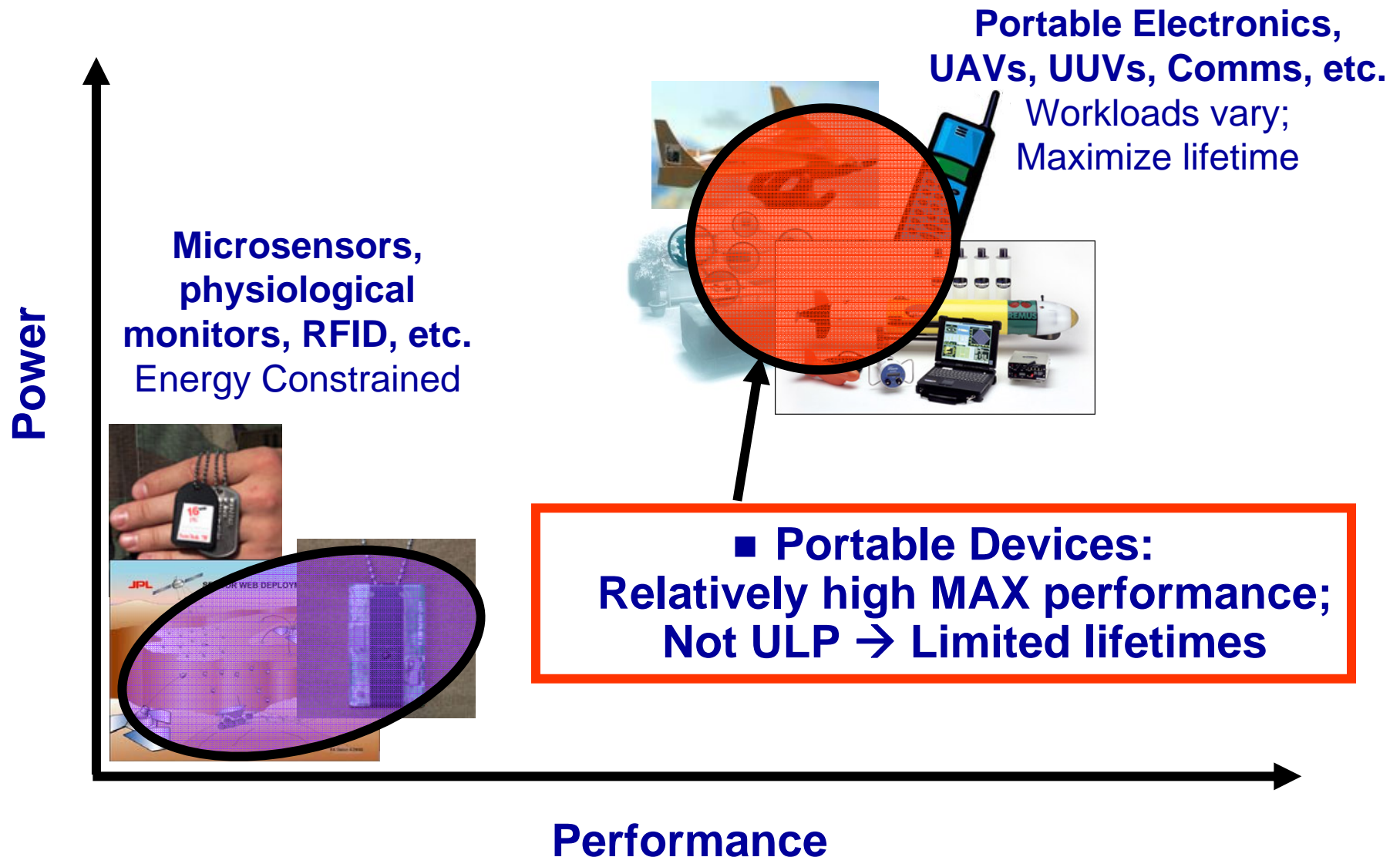
THESIS: Flexibility can help solve the key problems facing sub-threshold systems

- Energy / Performance Flexibility
- Hardware Flexibility
- System-Level Flexibility

“Low Power” Application Space



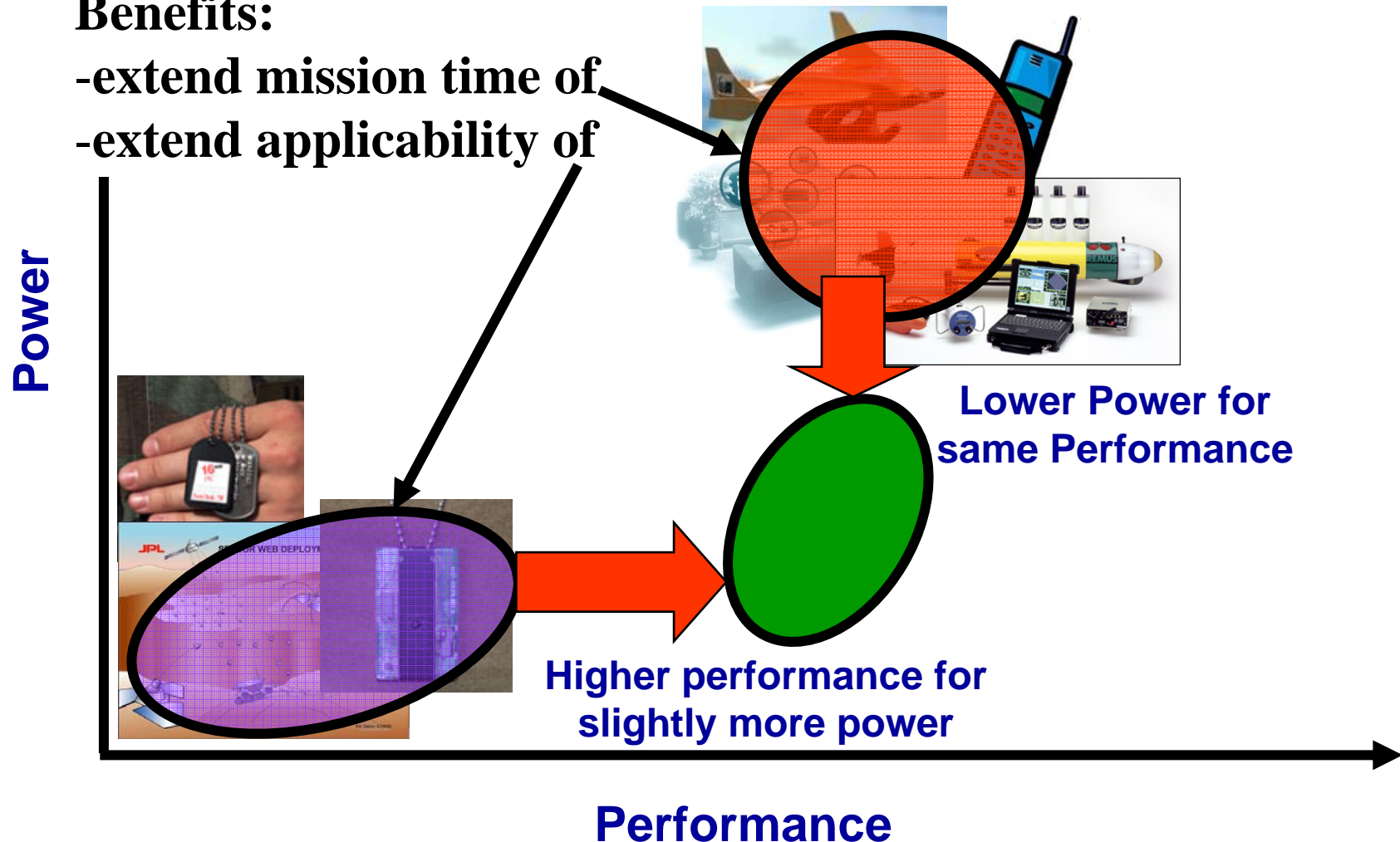
“Low Power” Application Space



Proposed Energy/Performance Flexibility

Benefits:

- extend mission time of
- extend applicability of



How will we do this?

- Key insight: Definition of Performance

Old definition: Fixed speed or throughput

**Accurate definition: Speed or throughput
required to get “the job” done**

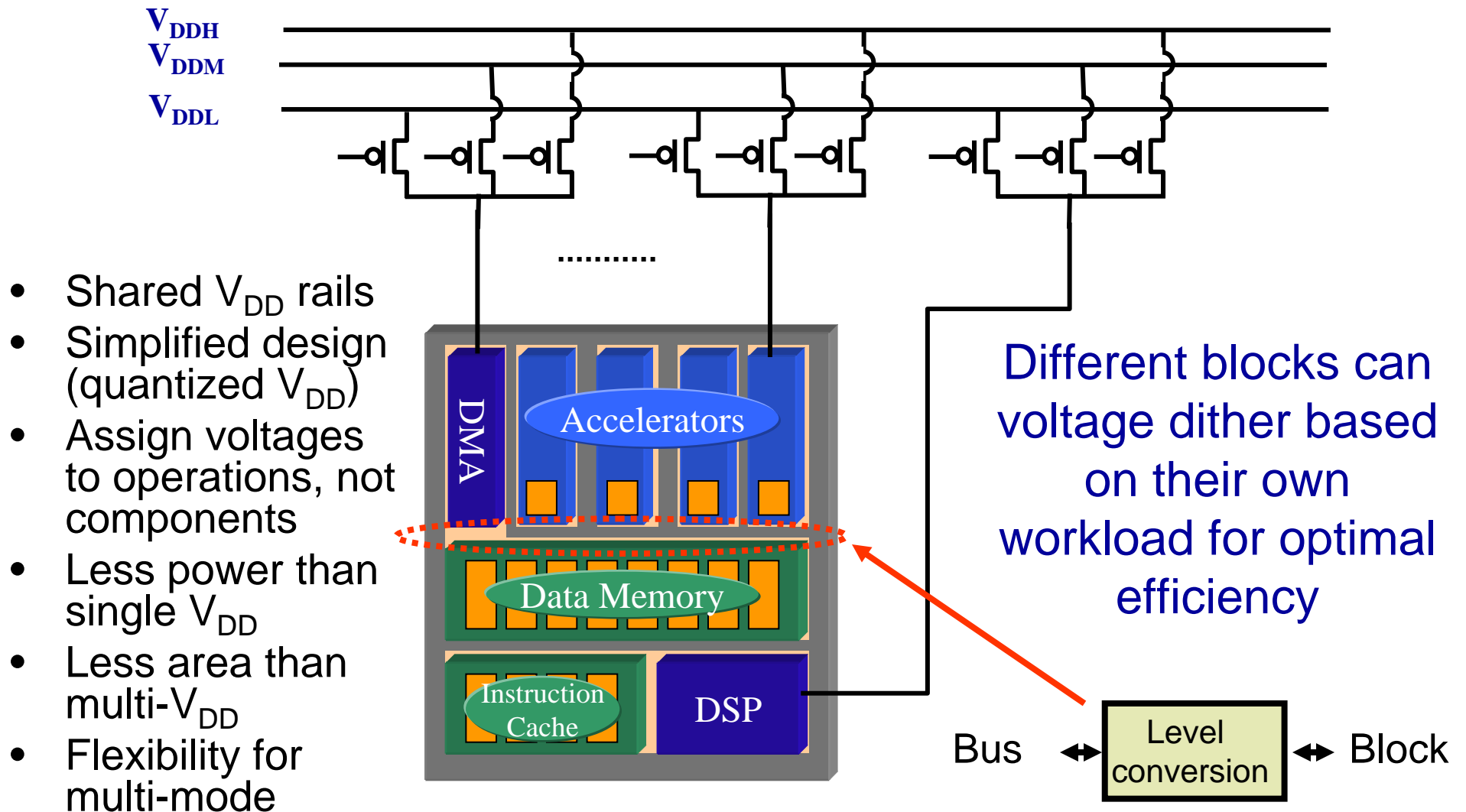
“The job” changes:

**→ a range of performance requirements
for a single app, depending on what
is going on**

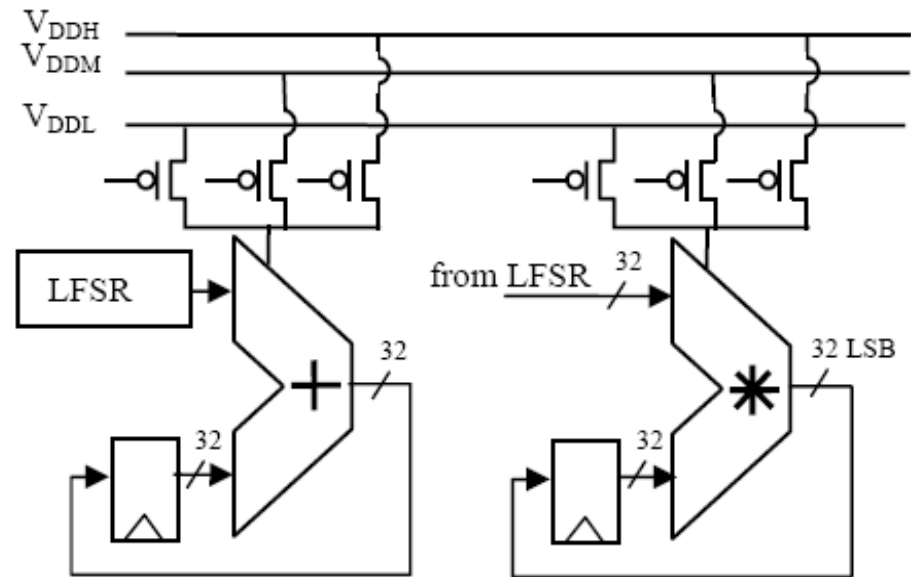
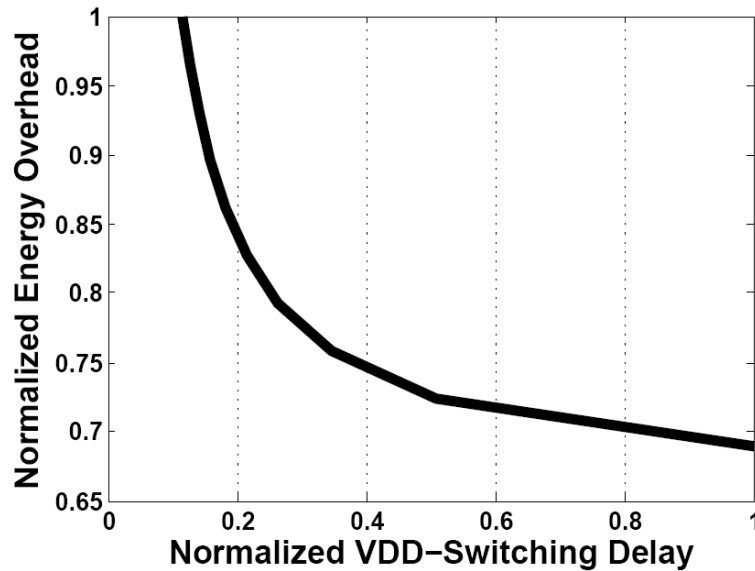
Proposed Approach

- Maximize efficiency of multi- V_{DD} design
 - Voltage is most effective knob
- Panoptic Dynamic Voltage Scaling (PDVS)
 - Multi- V_{DD} s (~2-4 voltage rails), local headers
 - Fully enables classical DVS
 - UDVS possible (hop to sub-threshold)
 - Finer *spatial* and *temporal* granularity
 - Multiple inherent power modes
 - Simple, low overhead implementation
 - LOTS of flexibility

Example System: Apply PDVS to ASIC



V_{DD}-switching energy



90nm Test Chip

Measured E overhead
to find number of
cycles at V_L to break even:
< 1!!

$$N_{BE} = \frac{(E_{High} - E_{Low})}{E_{switch}}$$

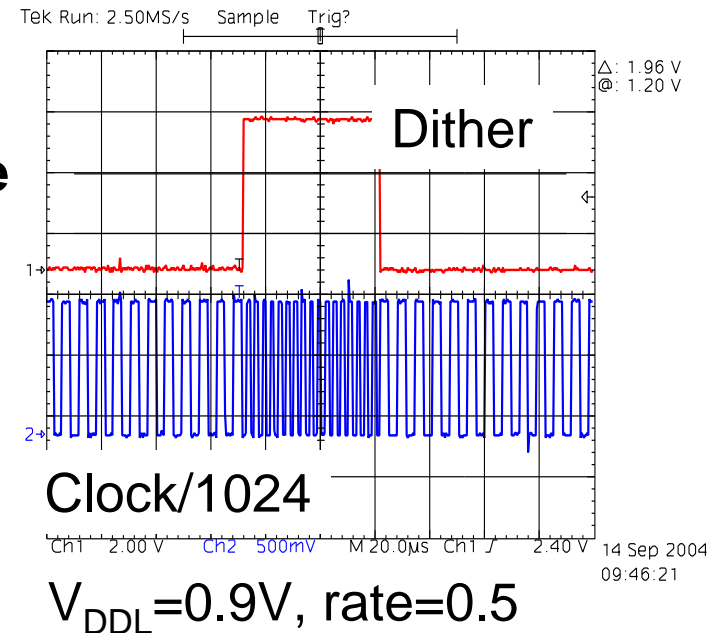
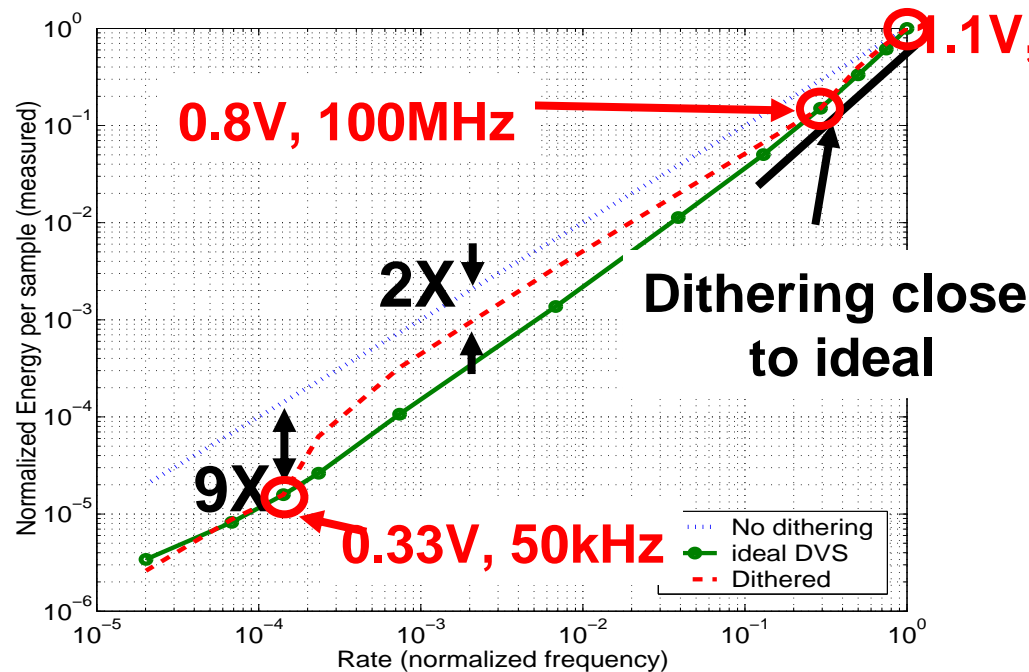
[ICCD, 2008]

Low Supply Voltage	Adder Break Even Cycles	Multiplier Break Even Cycles
0.9	0.689	0.436
0.8	0.579	0.408
0.7	0.607	0.263
0.6	0.721	0.328

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UDVS: ULP (Sub- V_T) Option

Dither during high performance operation and switch to sub-threshold minimum energy operation when speed is not important



Calhoun & Chandrakasan, "Ultra-Dynamic Voltage Scaling Using Sub-threshold Operation and Local Voltage Dithering in 90nm CMOS," ISSCC, 2005.

Outline

- Energy / Performance Flexibility
- Hardware Flexibility
- System-Level Flexibility

The Problem: Many ULP Applications

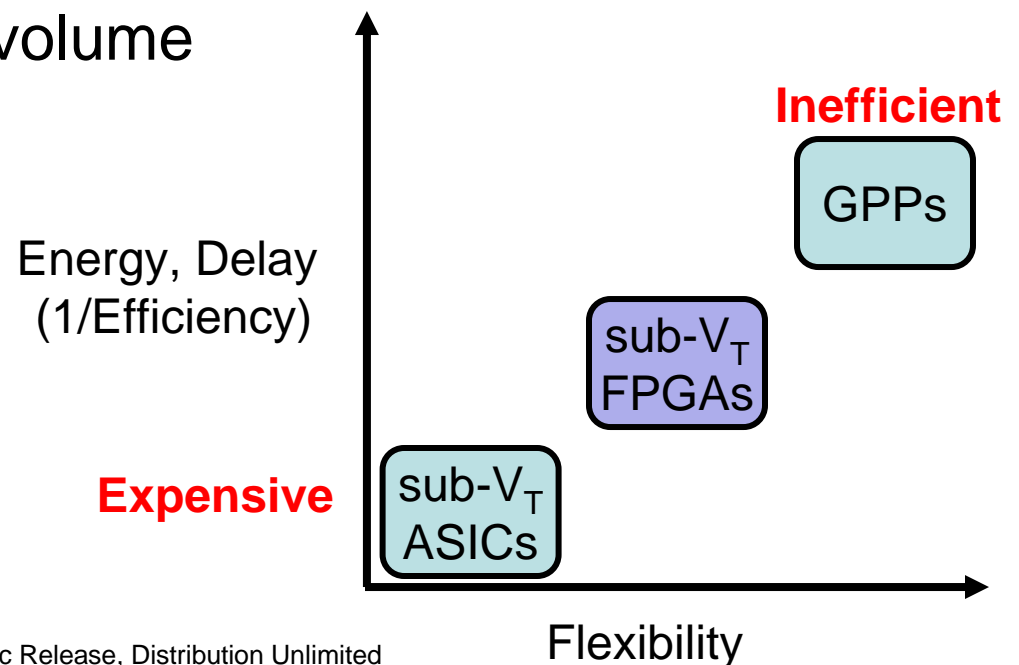
- Lots of apps (microsensors, RFID, tracking nodes, biotelemetry, micro-UAVs, hybrid insects, etc.)



- Need ULP (sub- V_T) for feasibility
- Economics: Often low volume

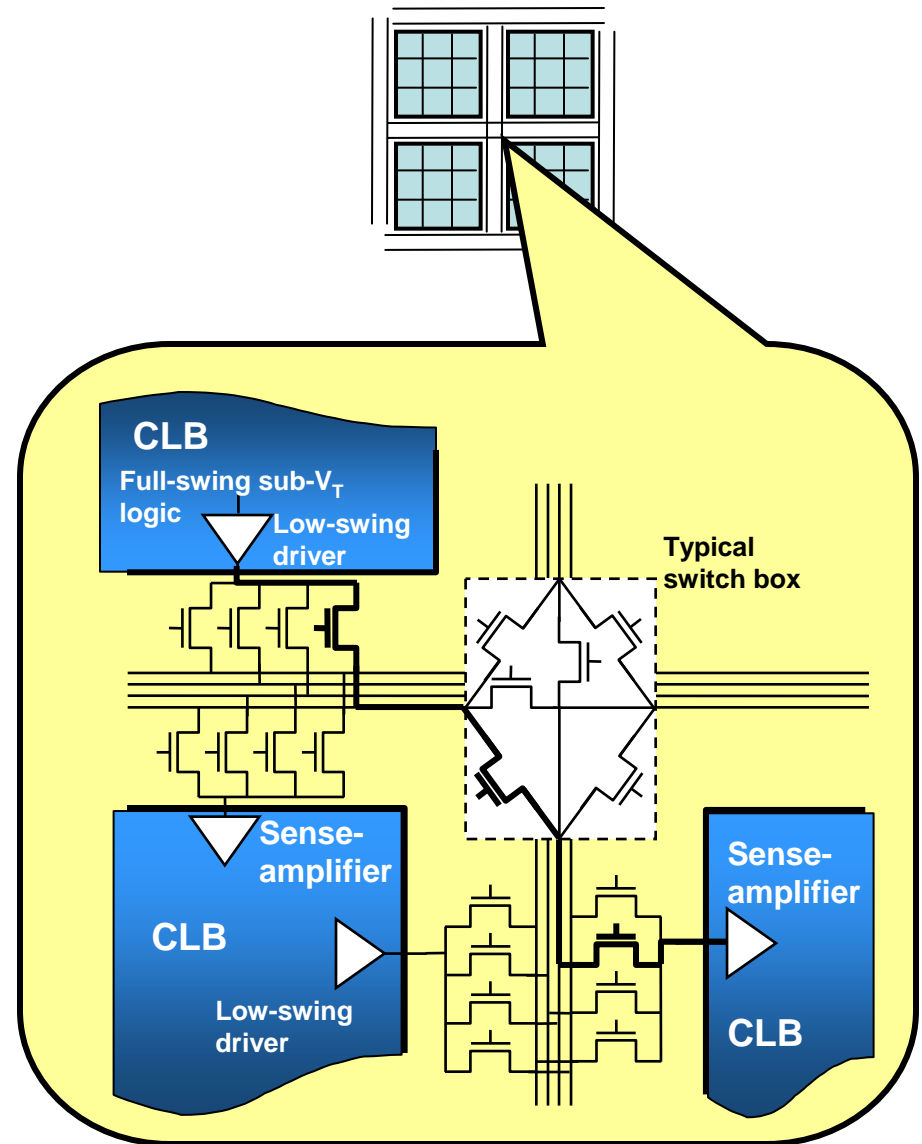
Sub- V_T FPGA:

- Flexible, portable
- Low time-to-deployment
- Mission-specific efficiency
- Low unit cost



Ultra Low Power FPGA

- **Challenges to sub- V_T FPGA**
- **Variation, low I_{on}/I_{off}**
- **Interconnect dominates delay and power**
- **Approach**
 - Low swing interconnect w/ sub-threshold sense amplifier
 - Regularity to reduce variation sources
 - Modified SRAM for config bits
- **Anticipated Result**
 - > 20X energy reduction
 - Tapeout spring 2009



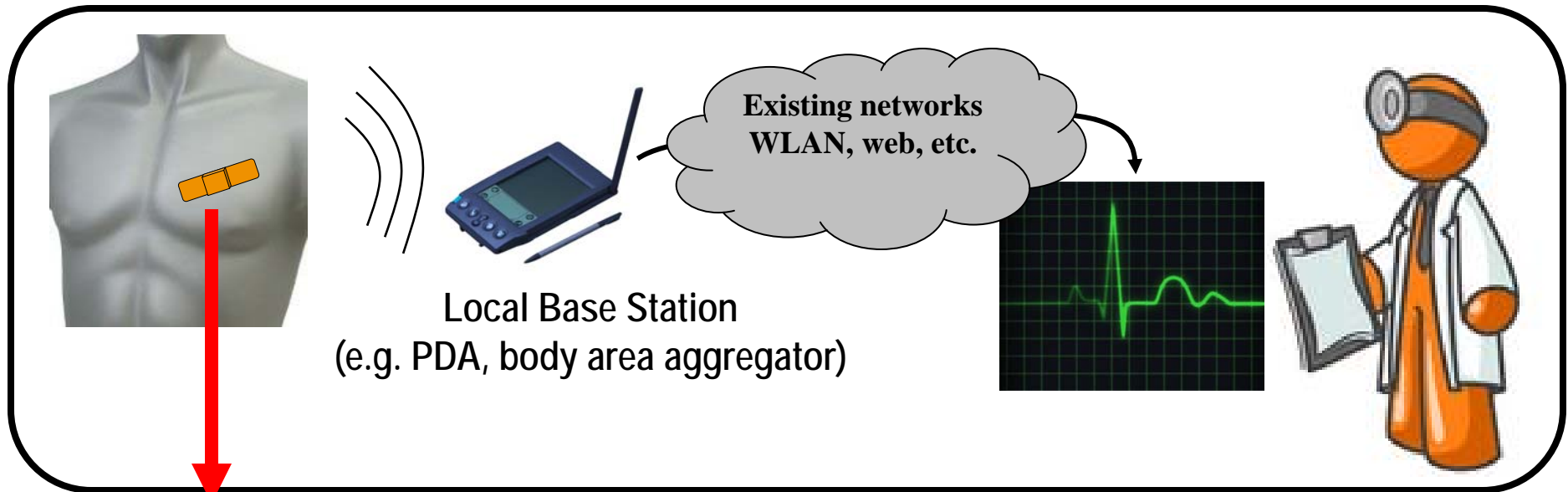
Outline

- Energy / Performance Flexibility
- Hardware Flexibility
- **System-Level Flexibility**

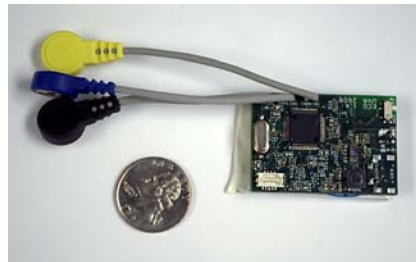
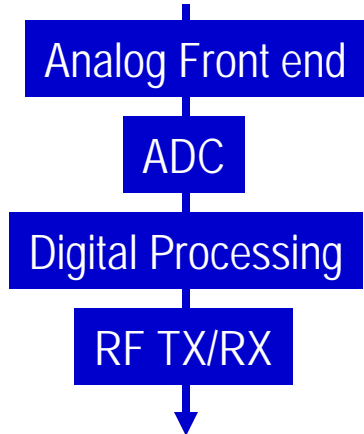
System Level Flexibility

- Must consider system power breakdown
- Radio often dominates
- Leverage ULP digital (e.g. pre-process to reduce wireless data rate)
- Example system: ECG on a band-aid

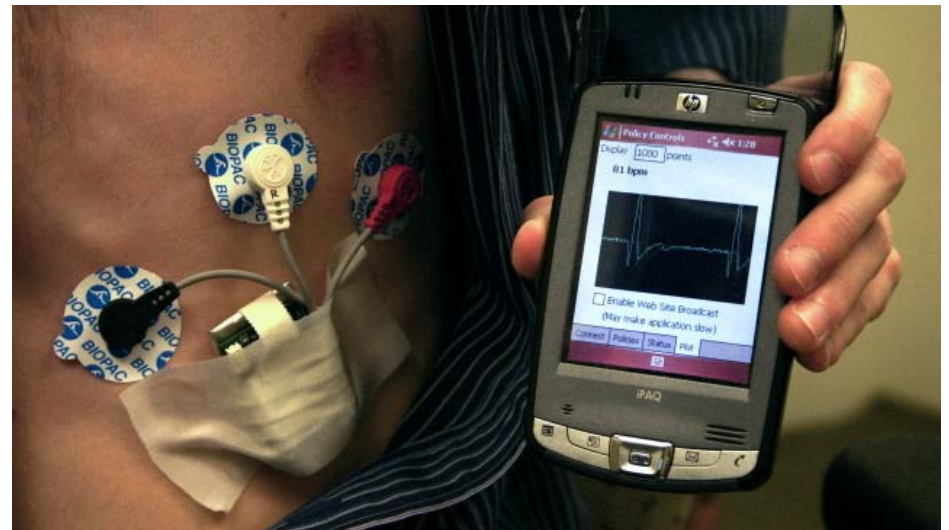
Example: ECG Monitoring System



ECG sensing "patch"



Discrete prototype

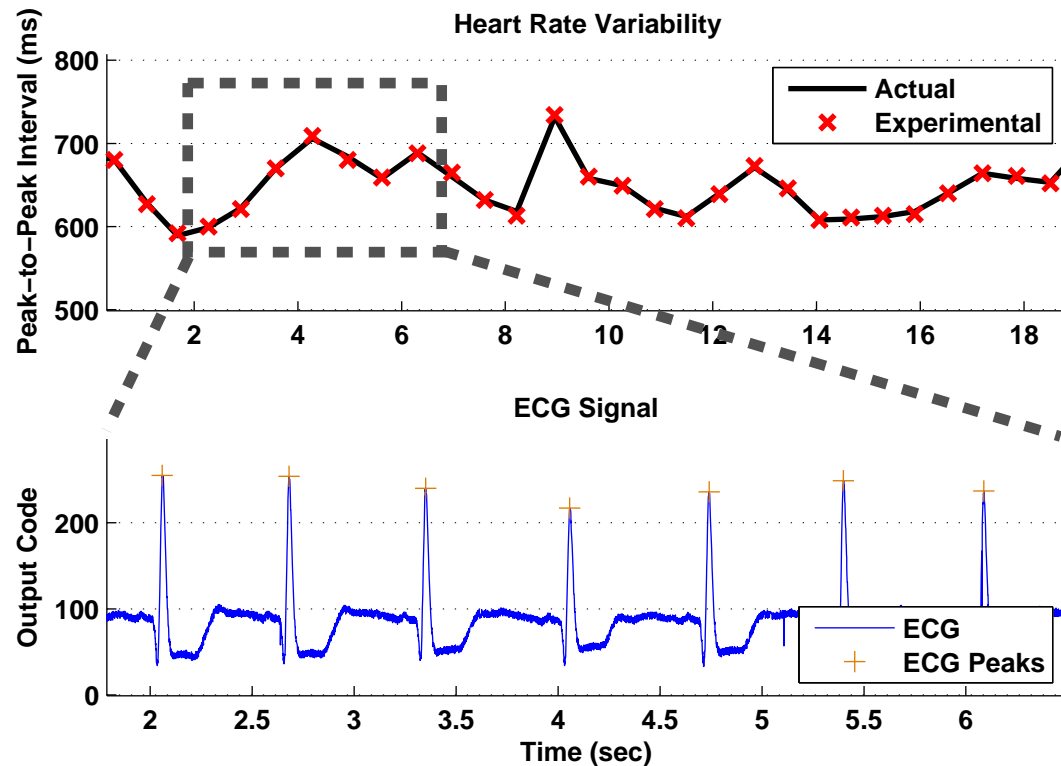
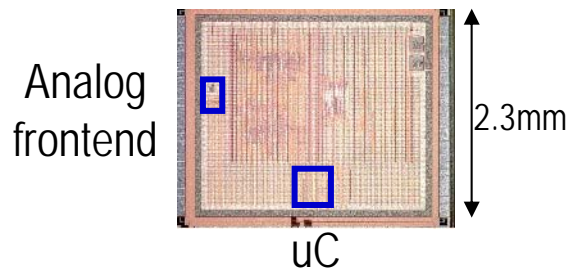
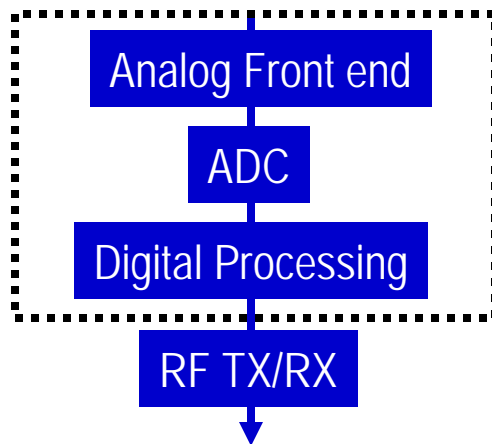


[with T. Blalock (UVA, ECE)]

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Mixed Signal ECG System on Chip

ECG sensing "patch"



Leverage Sub- V_T processing by re-partitioning tasks at system level

Heart rate computation cuts wireless data rate by 500X

[with T. Blalock (UVA, ECE)]

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Conclusions

- Flexibility solves key problems for sub- V_T systems
 - Energy/performance flexibility
 - Hardware flexibility
 - System flexibility
- Thank you! Any questions?

MICROSYSTEMS TECHNOLOGY OFFICE

MTO SYMPOSIUM

The logo for the Microsystems Technology Office (MTO) Symposium. It features the letters "MTO" in a large, bold, metallic font. The "O" is a circle containing a globe with the word "DARPA" on it. Circuit traces extend from the "M" and "O". Below "MTO" is the word "SYMPOSIUM" in a smaller, white, sans-serif font. The entire logo is set against a dark background with a reflection effect below it.

BUILDING THE FUTURE
FROM THE INSIDE OUT

The background of the poster is a collage of various technological and infrastructure images. On the left, there's a large satellite dish and a solar panel array. In the center, a ship's mast with various antennas and sensors is visible. On the right, there's a close-up of a building's exterior with a circular structure. The entire background is overlaid with a blue grid pattern and a network of lines and nodes, suggesting a global or interconnected system.

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